2020 Architecture Research with RISC-V and Chisel

Yunsup Lee
Andrew Waterman

Jonathan Bachrach, Scott Beamer, David Patterson, Krste Asanovic

Facilitating Credible Architecture Research

- Simulators are useful for measuring cycle counts—useless for power, area, cycle time
- But microarchitects must balance all of these!
- Need an end-to-end research methodology to close the feedback loop...
- ...but traditional HW design approaches with commercial ISAs are far too tedious

RISC-V ISA

- Straightforward 32-bit instruction encoding
- Supports compressed encodings and extended-length instructions

RISC-V Software Stack

- GCC 4.4 with Newlib C library
- “Proxy Kernel” to support POSIX calls by forwarding to a Linux host machine
- Coming soon, Linux and ROS/Tessellation

trainwreck: A RISC-V Prototype

- Simple 3-stage pipeline with decoupled data memory interface
- 64-bit fixed-point datapath, double-precision FP

Chisel

- Is a Hardware Construction Language
- Is not a Hardware Description Language: no un-synthesizable constructs
- Is type-safe and more expressive than Verilog
- Is embedded in Scala

Chisel Backends

Why a new ISA?

- Provide a realistic but open ISA that captures important details of commercial general-purpose ISA designs and that is suitable for hardware implementation.
- Provide a small but complete base ISA that avoids “over-architecting” for a particular microarchitecture style or implementation technology, but which allows efficient implementation in any of these.

Target Machine

- trainwreck core
- IS
- DS
- Refill Arbiter
- Outer Memory System

DEMO

- Hand written Trainwreck on FPGA & ASIC
- Chiseled Trainwreck on FPGA & ASIC