Overview

The vector-thread (VT) architecture can perform poorly on certain data-irregular codes.

We examined two hardware additions that significantly improve performance on certain classes of irregular code.

Vector Fragment Reconvergence

When vector fragments diverge, they stay divergent until the end of the vector fetch block.

This results in poor performance in common control sequences such as if statements within loops.

Although the special stacks are much more complex to implement, they incur no additional area cost and greatly improve the performance of divergent codes.

Memory Coalescer

When using microthread loads and stores, cache conflicts can degrade performance on certain common codes.

Sequential memory accesses of small strides can have cache conflicts so badly that they allow only one memory access per cycle.

Our memory coalescer allows a single memory request to satisfy memory requests of multiple lanes simultaneously. The vector memory unit dynamically compares memory addresses and stores word/halfword/byte select information in an extra buffer.